

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S167	39	((integrat\$ built\$1in) same (processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) same (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1) same (((non\$1volatile flash) near2 memory) EPROM EEPROM)) same (transmitter transceiver infra\$3 wireless)	USPAT	OR	ON	2004/10/26 16:49
S154	61	(((((processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) same (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1)) same (non\$1volatile memory)) same (integrat\$3 near2 circuit)) same program\$5) same (transmitter transceiver infra\$3 wireless)	USPAT	OR	ON	2004/10/26 16:49
S166	1	"25".ab.	USPAT	OR	ON	2004/10/26 16:48
S165	25	((integrat\$ built\$1in) same (processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) same (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1) same (((non\$1volatile flash) near2 memory) EPROM EEPROM)) and "716"/\$.ccls.	USPAT	OR	ON	2004/10/26 16:48
S164	11	((integrat\$ built\$1in) same (processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) same (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1) same (((non\$1volatile flash) near2 memory) EPROM EEPROM)) and "326"/\$.ccls.	USPAT	OR	ON	2004/10/26 16:48
S163	25	((integrat\$ built\$1in) same (processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) same (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1) same (((non\$1volatile flash) near2 memory) EPROM EEPROM)) and "710"/\$.ccls.	USPAT	OR	ON	2004/10/26 16:48

S16 2	1	"25".clm.	USPAT	OR	ON	2004/10/26 16:47
S16 1	244	(integrat\$ built\$1in) same (processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) same (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1) same (((non\$1volatile flash) near2 memory) EPROM EEPROM)	USPAT	OR	ON	2004/10/26 16:47
S16 0	0	(integrat\$ built\$1in) near4 (processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) near4 (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1) near4 (((non\$1volatile flash) near2 memory) EPROM EEPROM)	USPAT	OR	ON	2004/10/26 16:47
S15 9	2	(((((processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) same (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1)) same (non\$1volatile memory)) same (integrat\$3 near2 circuit)) same program\$5) same (transmitter transceiver infra\$3 wireless)) and "716"/\$.ccls.	USPAT	OR	ON	2004/10/26 16:40
S15 8	3	(((((processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) same (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1)) same (non\$1volatile memory)) same (integrat\$3 near2 circuit)) same program\$5) same (transmitter transceiver infra\$3 wireless)) and "326"/\$.ccls.	USPAT	OR	ON	2004/10/26 16:34
S15 7	9	(((((processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) same (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1)) same (non\$1volatile memory)) same (integrat\$3 near2 circuit)) same program\$5) same (transmitter transceiver infra\$3 wireless)) and "710"/\$.ccls.	USPAT	OR	ON	2004/10/26 16:34
S15 6	1	"18".clm.	USPAT	OR	ON	2004/10/26 16:34

S15 5	1	"18".ab.	USPAT	OR	ON	2004/10/26 16:34
S15 3	564	(((((processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) same (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1)) same (non\$1volatile memory)) same (integrat\$3 near2 circuit)) same program\$5	USPAT	OR	ON	2004/10/26 16:33
S15 2	683	(((((processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) same (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1)) same (non\$1volatile memory)) same (integrat\$3 near2 circuit))	USPAT	OR	ON	2004/10/26 16:32
S15 1	39	"10".clm.	USPAT	OR	ON	2004/10/26 16:31
S14 7	60	"10".ab.	USPAT	OR	ON	2004/10/26 16:31
S15 0	8	"10".ab. and "716"/\$.ccls.	USPAT	OR	ON	2004/10/26 16:30
S14 9	13	"10".ab. and "326"/\$.ccls.	USPAT	OR	ON	2004/10/26 16:30
S14 8	12	"10".ab. and "710"/\$.ccls.	USPAT	OR	ON	2004/10/26 16:30
S14 6	3133	((processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) same (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1)) same (non\$1volatile memory)	USPAT	OR	ON	2004/10/26 16:30
S14 5	7410	(processor micro\$1processor micro\$1controller dsp (digital near2 signal near2 processor)) same (PLD\$1 PAL\$1 FPLA\$1 CPLD\$1 EPLD\$1 EEPLD\$1 LCA\$1 FPGA\$1)	USPAT	OR	ON	2004/10/26 16:29